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の回路図である。

(图6)

從來の保護回路及びその保護回路が適用される回路構造の回路図である。

(图7)

本回路における負荷の電源オフ時のサージ電流等の様子を示す図である。

解説

主回路

図面
FIG. 1

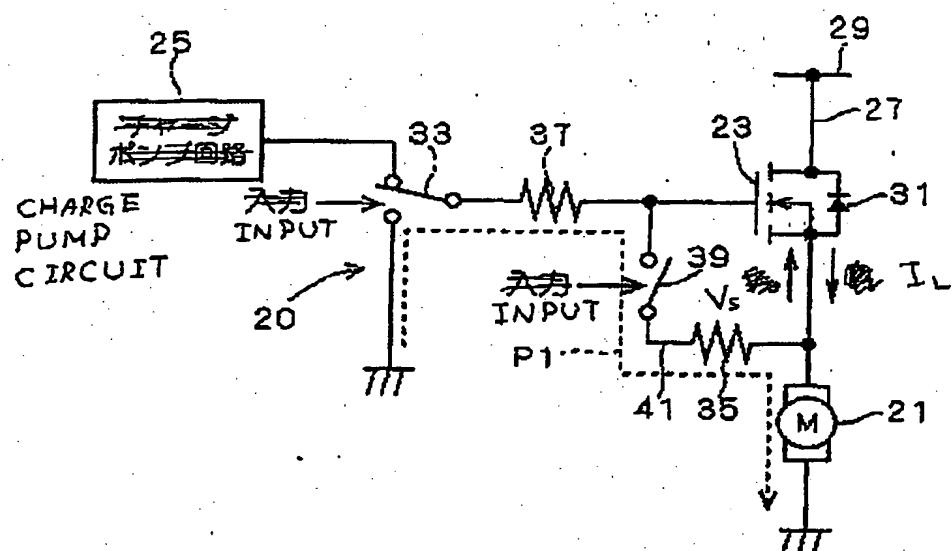


図2

H51-167124 M/KT

~167125

US. DE

FIG. 2

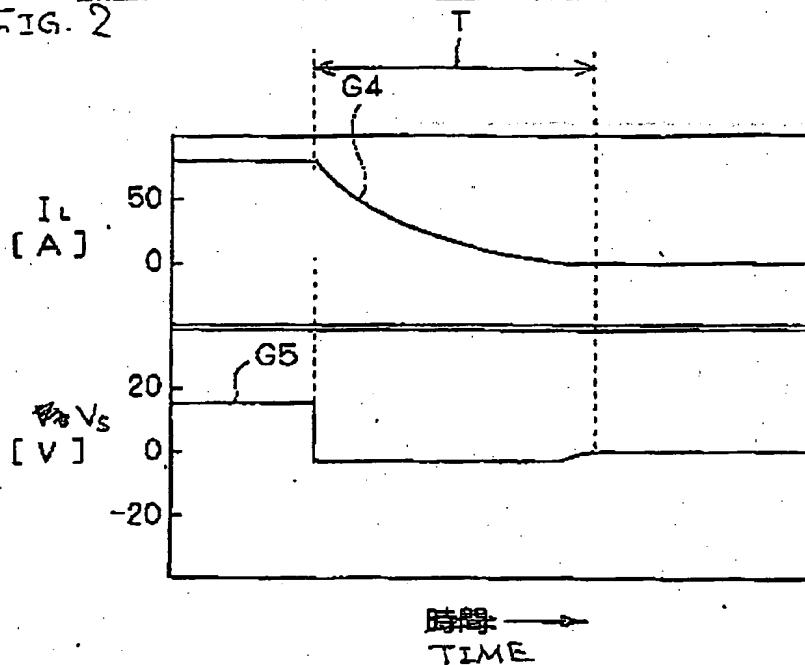


FIG. 3

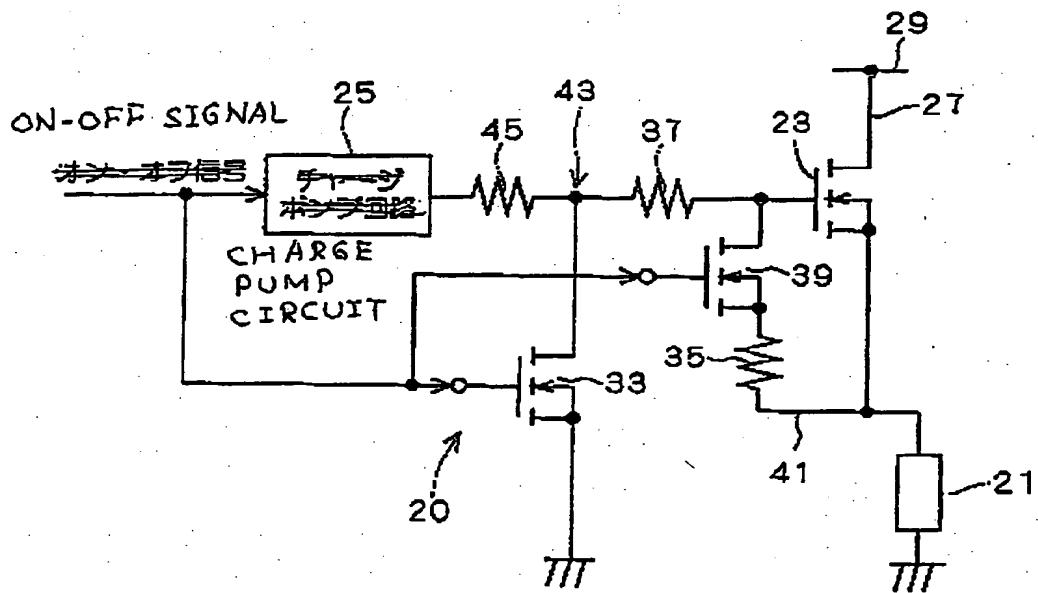


FIG. 4

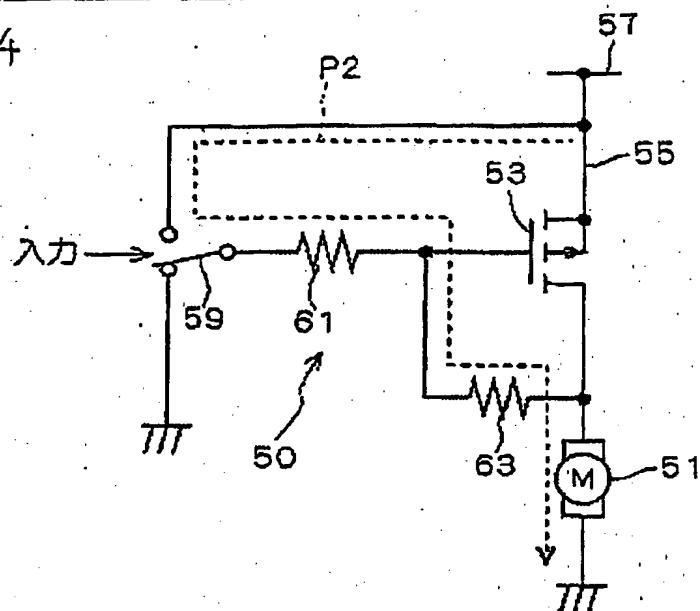


FIG. 5

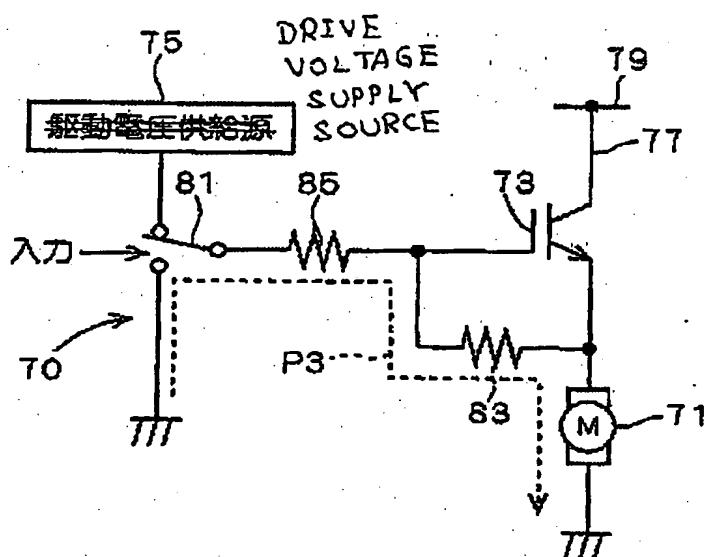


FIG. 6

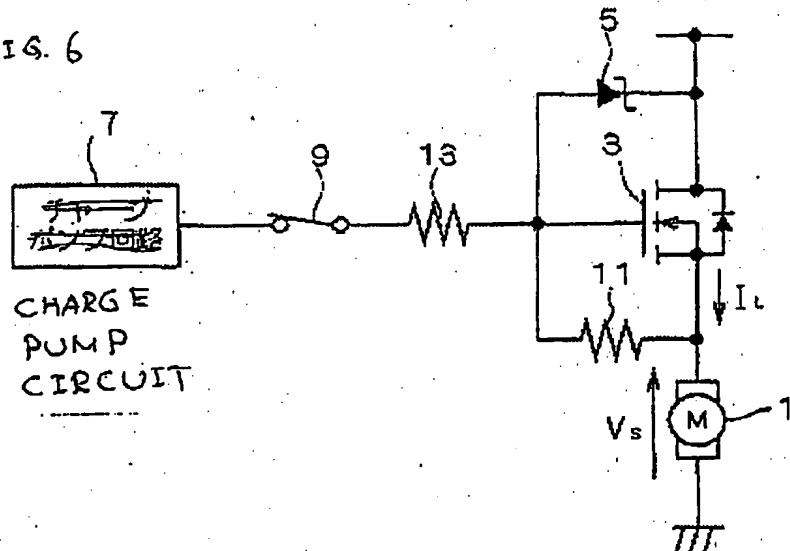
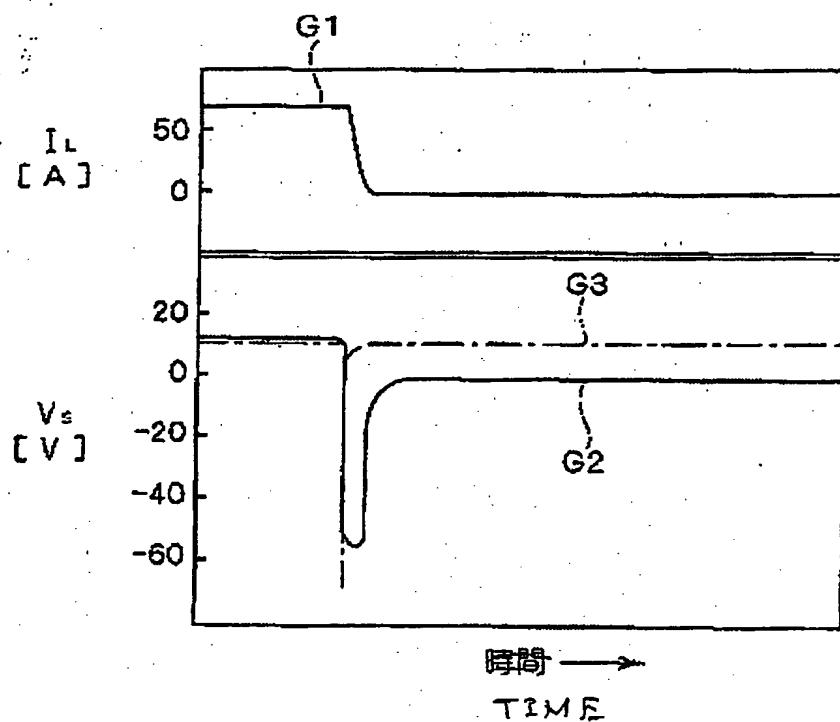


FIG. 7



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【要約】